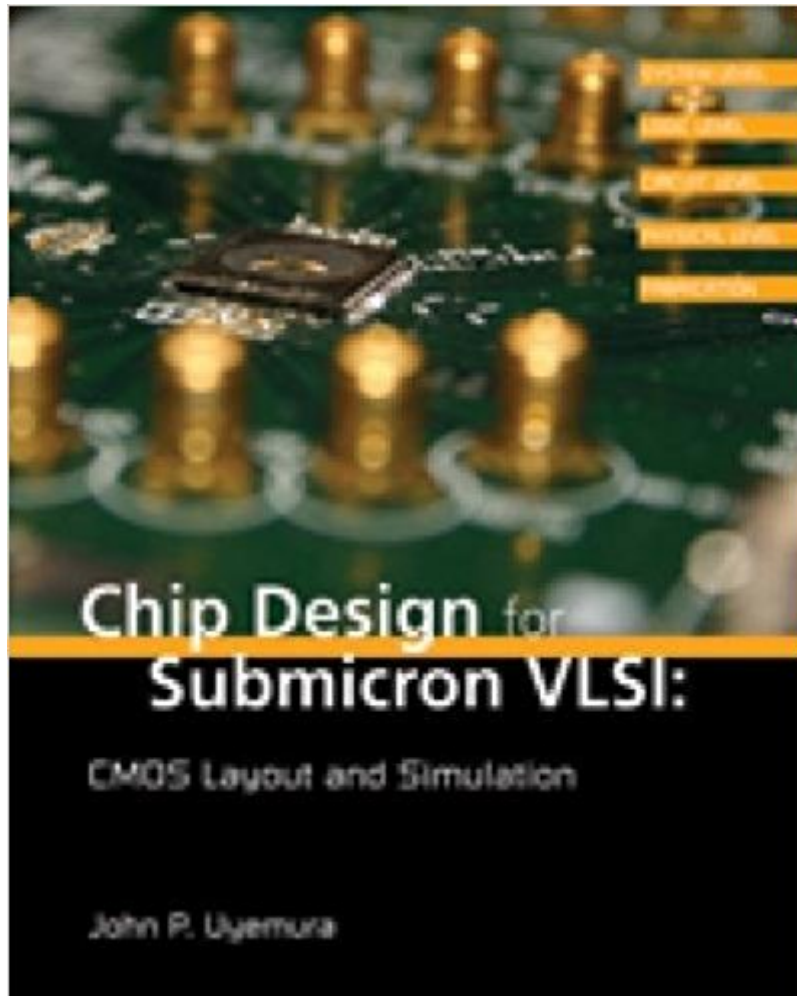




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Chip Design For Submicron VLSI: CMOS Layout And Simulation



Synopsis

The text is organized around first introducing the global view of digital integrated circuit design, VLSI and design automation, and then sequentially developing the topics from the materials and devices level, up through the circuits and then system level. This mirrors the structural hierarchy of the chip design field itself. While building a solid foundation and reference for the chip design, it integrates the discussion with hands-on examples of the design automation software, included in the book, to illustrate not only the layout and simulation concepts, but also how an industry designer would put them into practice. Both theory and application are effectively integrated into a cohesive treatment of the subject and art of chip design.

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John P. Uyemura is Professor of Electrical and Computer Engineering, late of Georgia Institute of

Technology.

The "Chip Design for Submicron VLSI" written by John Uyemura was like brand new, even though I was buying it as a used book from . My experience with was always very good. They are very prompt in delivering the items in time. Many many thanks for the good work. I am very happy to recommend to anyone.

I would like to write about "Chip Design for Submicron VLSI:CMOS Layout and Simulation" book (2006 ed.,THOMSON), written by John P. Uyemura.General : As the author mentioned that the book is a basic introduction to submicron CMOS designs,you will find the book contents organized into short chapterswith a level of details that one can study and understand within a short period.The software(Microwind and Dsch) that comes with the book is a nice tool to start learning CMOS VLSI layout and simulation.It would be best to practice asyou read and understand each section or topic.You can learn much from hands on by doing your own version of layouts or circuits for simulation.Each figure of a layout shown in the book is usually large enough to clearly see the details.Thus, you can try to recreate your own layout as seen fromthe figure.An important note about using Dsch program should be given here.In a Dsch schematic,you cannot name an input with "/" as a part of the name,if you planto compile the circuit to Verilog code,otherwise you will get a Compile Verilog file error.Author's Writing Style: The author is one of well known writers in the field of CMOS VLSI circuits and systems.If you have seen this book,and maybe also some other bookswritten by him in a book store,you probably agree that his books are quite easy to read due to a clear and concise organization and a way he usuallywrites to convey information and present ideas.Key words are usually highlighted in each section.This helps for finding related explanation or specificconcepts and ease of reviews.Errata: I found only a few(might be sent to publisher), the book is well written.The information here about the content should help anyone who feel interested to have some ideas about how much the book is directly useful for his or her application or learning interest.Contents: 406 pages of content,a small book. Each chapter contains a short list of References and a few excercise problems at the end of each chapter.- Chapter 1 Installing the Microwind Software (15 pages)- Chapter 2 Views of a Chip--Layers and Patterns (21 pages)- Chapter 3 CMOS Technology--A Basis for Design(27 pages)- Chapter 4 Using a Layout Editor--Fundamental Concepts (18 pages)- Chapter 5 CMOS Design Rules--Guidelines for Layout (23 pages)- Chapter 6 MOSFETs--Operation and Analytical Models (26 pages)- Chapter 7 MOSFET Modeling with SPICE (23 pages)- Chapter 8 CMOS Logic Gates--Design and Layout (41 pages)-

Chapter 9 Standard Cell Design--Layouts and Wiring (22 pages)- Chapter 10 Storage Elements--Design and Layout (15 pages) - Chapter 11 Dynamic Logic Circuits--Basic Principles (14 pages)- Chapter 12 Interconnect--Routing and Modeling (20 pages)- Chapter 13 System Layout--Physical Design of the Chip (23 pages)- Chapter 14 SOI Technology--Introduction to Basics (12 pages)- Chapter 15 Digital System Design 1--The Dsch Program (28 pages)- Chapter 16 Digital System Design 2--Design Flow Examples (22 pages)- Chapter 17 Capacitors and Inductors On-Chip Passive Elements (12 pages)- Chapter 18 Analog CMOS Circuits Layout Basics (17 pages) - Appendix A Microwind Command Summary (8 pages) The appendix contains a summary of the Menu options in Microwind, each pointed with an arrow and short description. A.1 File- the group of commands for all file operations; A.2 View- commands to control the appearance of layout drawing; A.3 Edit- commands to do basic object manipulations and custom placement of rectangles; A.4 Simulate- commands for SPICE simulations, 2D and 3D viewers; A.5 Compile- two commands for automated design; A.6 Analysis- DRC, Measurement tool and Parametric Analysis (some versions); A.7 Help- access to online versions of design rules and reference manual; A.8 Menu Bar- shortcut buttons for major operations, both left-side buttons and right-side buttons shown; A.9 Other Screens- refer to the online Help function and User's Manual.- Appendix B Microwind CMOS Technology Files (11 pages) Explanation about parameter listing and parameters defined in .rul files. The sample listing is from the cmos018.rul file. The values contained in the file are, for example, layer information, design rules, device parameters, parasitics, CIF layer definitions, data for 2D and 3D views.----Sittinart N.

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